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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,724	02/10/2004	Masatoshi Yasutake	S004-5210	3824

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ADAMS & WILKS
17 BATTERY PLACE
SUITE 1231
NEW YORK, NY 10004

EXAMINER	
JEFFERSON, QUOVAUNDA	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,724	YASUTAKE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 36-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 36-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claims 47 and 48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no description in the specification as originally filed of "sample chip with a wall surface is formed with stepped portions due to difference in the materials of the multi-layered structure of the sample". There is only seen description of "sample chip with a wall surface is formed with stepped portions".

2. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "upward" in claim 37 is a relative term, which renders the claim indefinite. The term "upward" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Examiner is unsure as to what direction or coordinate system is being referred to as "upward". Does upward mean that the etched wall sample face opposite the face that is being placed onto the stage for observation or does "upward" refer to the etched sample wall faces towards the instrument in which it is being observed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1, 47 and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirose, US Patent 6,826,971 (herein referred to as Hirose'971).**

5. Regarding claim 1, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of by irradiating the sample with a focused ion beam to form a sample chip having a wall surface with stepped potions formed (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, line 18-23), and a third step of observing a the wall surface of the taken sample chip with a scanning probe microscope (SPM) (column 7, line 55).

6. Regarding claim 47, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of providing a sample having a multi-layered structure made of different materials (column 1, lines 51-55), irradiating the sample with a focused energy beam to form a sample chip while a wall surface of the sample chip is gas-assist-etched so that the wall surface is formed with stepped portions due to differences in the materials of the multi-layered structure of the sample (see column 3, lines 60-67 and column 4, lines 1-17 where tungsten film, the stepped portion of the sample chip, is installed on the chip using tungsten gas when the gas is

used with the focus ion beam), taking out the sample chip from the sample (column 5, lines 18-23), and observing the wall surface of the sample chip having the stepped portions with a scanning probe microscope (column 7, line 55).

7. Regarding claim 48, Hirose'971 further teaches the focused energy beam is a focused ion beam (abstract).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 36, 37, 40, 43, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose, US Patent 6,826,971 (referred to as "Hirose'971") in view of Hitachi LTD, Patent Abstract of Japan 05-052,721 (referred to as "Hitachi").**

10. Regarding claim 36, Hirose '971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of the

sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of picking-up the sample chip from the sample (column 5, line 18-23), and a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55).

Hirose'971 fails to teach a third step of irradiating a wall surface of the sample chip with a second focused energy beam to thereby etch the wall surface.

However, Hitachi teaches a third step of irradiating a wall surface of the sample chip with a second focused energy beam to thereby etch the wall surface (abstract, [0018]) first, as a means of forming a separated sample directly after the formation of an FIB etched sample, which can be inserted into various kinds of analyzing devices differently with respect to the FIB etched sample and second, by teaching the reworking of the FIB etched sample into a configuration that is suitable for analysis.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hitachi with that of Hirose'971 because a smaller separated sample can be inserted into various kinds of analyzing devices differently with respect to

sample 2 or the FIB sample may be re-etched into an optimal shape for observation and analysis.

11. Regarding claim 37, Hirose'971 teaches the second step further comprises the step of securing the sample chip to a sample chip holder **25** after the sample chip is picked-up from the sample (with microprobers **22)** so that the wall surface of the sample chip etched in the third step (column 5, lines 57-61) and observed in the fourth step faces in an upward direction (In figure 10, the defect can be viewed from 53a in a TEM or SEM microscope, showing a view as shown in figure 11 as defect **3**)

12. Regarding claim 40, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of the sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column **4**, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, line 18-23), a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55), and a fifth step of irradiating the observed wall surface of the sample chip with the first focused energy beam to thereby to etch the observed wall surface (to further explain, Hirose'971 teaches one method of observing the sample is through a

TEM type of microscope. Hirose'971 explains that if necessary, the sample can be thinned using the focus ion beam. Therefore, one of ordinary skill in the art would know that after a first observation using a TEM or SPM, if the sample is too thick to observe, the sample would need to be thinned, using a FIB and that the sample can be thinned by irradiating the observed wall surface and/or any wall surface that is deemed necessary, then observing the sample again using a TEM or SPM), and a step of repeating the third to fifth steps a preselected number of times (which can be done by repeat observing and irradiating to thin down the sample).

Hirose'971 fails to teach the third step of irradiating a wall surface of the sample chip with a second focused energy beam thereby to etch the wall surface.

Hitachi teaches the third step of irradiating a wall surface of the sample chip with a second focused energy beam thereby to etch the wall surface (abstract, [0018]) first, as a means of forming a separated sample directly after the formation of an FIB etched sample, which can be inserted into various kinds of analyzing devices differently with respect to the FIB etched sample and second, by teaching the reworking of the FIB etched sample into a configuration that is suitable for analysis.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hitachi with that of Hirose'971 because a smaller separated sample can be inserted into various kinds of analyzing devices differently with respect to

sample 2 or the FIB sample may be re-etched into an optimal shape for observation and analysis.

13. Regarding claim 43, Hirose'971 teaches method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a preselected portion of a sample and an area surrounding the preselected portion of the sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, lines 18-23a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55), a fifth step of irradiating the observed wall surface of the sample chip with the first focused energy beam to thereby to etch the observed wall surface(to further explain, Hirose'971 teaches one method of observing the sample is through a TEM type of microscope. Hirose'971 explains that if necessary, the sample can be thinned using the focus ion beam. Therefore, one of ordinary skill in the art would know that after a first observation using a TEM or SPM, if the sample is too thick to observe, the sample would need to be thinned, using a FIB and that the sample can be thinned by irradiating the observed wall surface and/or any wall surface that is deemed necessary, then observing the sample again using a TEM or SPM) and a step of repeating the fourth

and fifth steps a reselected number of times (which can be done by repeat observing and irradiating to thin down the sample).

Hirose'971 fails to teach a third step of irradiating a wall surface of the sample chip with a second focused energy beam thereby to etch the wall surface.

Hitachi teaches teach a third step of irradiating a wall surface of the sample chip with a second focused energy beam thereby to etch the wall surface (abstract, [0018]) first, as a means of forming a separated sample directly after the formation of an FIB etched sample, which can be inserted into various kinds of analyzing devices differently with respect to the FIB etched sample and second, by teaching the reworking of the FIB etched sample into a configuration that is suitable for analysis.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hitachi with that of Hirose'971 because a smaller separated sample can be inserted into various kinds of analyzing devices differently with respect to sample 2 or the FIB sample may be re-etched into an optimal shape for observation and analysis.

14. Regarding claim 46, Hirose'971 and Hitachi fail to teach the step of forming the sample chip with a rectangular parallelepiped shape in an asymmetric form to facilitate identification of the wall surface of the sample chip in the fourth step. However, it would

have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

15. **Claims 38, 39, 41, 42, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose'971 and Hitachi as applied to claim 36 above, and further in view of Mizumura, US Patent 5,825,035**.

16. Regarding claims 38, 41, and 44, while Hitachi teaches the use of second focused energy beam, Hirose'971 and Hitachi fail to teach a focus energy beam is an argon ion beam.

Mizumura teaches the focus energy beam using an argon beam (column 9, lines 26-35), with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of Hirose'971 and Hitachi because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals

17. Regarding claims 39, 42, and 45, Hirose'971 teaches the first step includes the step of processing the sample chip to form stepped portions in the wall surface of the sample chip (Note: it is generally known in the art that when a sample is etched from a wafer or a chip, the sample is going to have a wall surface with stepped portions because a sample that is etched from a bigger sample will always be a 3 dimensional sample with a thickness, thereby creating a wall surface and stepped portion, irregardless of the geometry of the smaller sample).

Response to Arguments

1. Applicant has respectfully traversed the prior art of record in the final office action dated June 29, 2006. Applicant's Arguments with respect to claims 1, 47, and 48 have been reconsidered and are not persuasive.

2. With regards to claim 1, Applicant argues that Hirose'971 does not meet the explicit limitations as set forth by the claim. In particular, Applicant recited that Hirose fails to meet the limitation of formation of a sample chip having a wall surface formed with stepped portions by an etching step, which requires irradiating the sample with a focus ion beam. In addition, Applicant contends that Hirose fails to teach observing the wall surfaces of a sample chip with stepped portions with a scanning probe microscope.

3. In response to these arguments, Hirose does indeed teach these limitations. In the last office action, the Examiner did point out that the sample chip did have a stepped portion due to the tungsten film **23** that was added due to the microprobe. However, as shown in figures 7 and 9 of Hirose, a sample is taken from the original chip or wafer by irradiating a focus ion beam upon an area that contains the defect and the area surrounding the defect. The sample that is extracted is in the geometric shape of a block, which can be described as having several wall surfaces and several stepped portions. Examiner also points out that the drawings of the Applicant also show this

same 3-dimension step block sample as the "sample chip having a wall surface formed with stepped portion".

4. Also, Hirose teaches that the sample, which is placed onto a support base for analysis of said sample chip with stepped portion. Hirose then goes on to teach that this analysis may be conducted by several different instruments, such as a scanning electron microscope (SEM), a transmission electron microscope (TEM), scanning ion electroscope (SIM), and a scanning probe microscope (SPM), all of which are well-known in the art, See column 1, line 61; column 6, lines 18-20; and column 7, lines 40-57.

5. Therefore, Hirose meets the limitations as set forth in claim 1 and the rejection of claim 1 in view of Hirose'971 is deemed proper.

6. With regards to claims 47 and 48, Applicant again argues that Hirose does not meet the limitations of the sample chip with the stepped profile and observation with a scanning probe microscope. In addition, Applicant argues that Hirose fails to teach a stepped profile due to the difference in materials of a sample having a multi-layered structure.

7. In response to these arguments, Examiner again points out that Hirose does indeed teach the limitation of a sample chip with a stepped profile as stated before. As

shown in figures 7-9, this sample, which has a multi-layered structure, is taken from the original chip or wafer by irradiating a focus ion beam upon an area that contains the defect and the area surrounding the defect. The sample that is extracted is in the geometric shape of a block, which can be described as having several wall surfaces and several stepped portions, which is exactly the same as the drawings as shown by Applicant. Also, Hirose teaches that the sample, which is placed onto a support base for analysis of said sample chip with stepped portion, with the SPM being one of several instruments well-known in the art for sample analysis, as stated previously.

8. In addition, while the claim recites the limitation that sample chips with a wall surface formed with stepped portions is due to the difference in the materials of the multi-layered structure, Applicant has failed to recite this limitation in the specification, thereby adding new matter into the claim. Despite that, Examiner would like to point out that it is generally known in the art that when a sample is etched from a wafer or a chip, the sample is going to have a wall surface with stepped portions because a sample that is etched from a bigger sample will always be a 3 dimensional sample with a thickness, thereby creating a wall surface and stepped portion, irregardless of the geometry of the smaller sample.

9. Therefore, Hirose meets the limitation as set forth in claims 47 and 18 and the rejection of these claims in view of Hirose'971 is deemed proper.

10. Applicant's arguments, see pages15-16, filed December 1, 2006, with respect to claims 36-46 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando L. Toledo
Primary Examiner
Art Unit 2823

QVJ